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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/281,358	03/30/1999	ROGER PANICACCI	08305/031001	7144

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Micron Technology, Inc.
c/o Tom D'Amico
Dickstein, Shapiro, Moran & Oshinsky
2101 L Street, NW
Washington, DC 20037-1526

EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2615	19

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/281,358	PANICACCI, ROGER	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-8* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 3/18/2204 with respect to claims 1-3 and 8 have been fully considered but they are not persuasive.

Regarding claim 1, the Applicant argues that Gowda fails to teach or suggest associating an A/D converter with multiple registers since each A/D converter 40 is associated with a single associated register 42 (remarks, pages 5 and 6). However, claim 1 does not require each A/D converter includes multiple registers. It is seen that "a plurality of associated storage elements" appear not necessarily belong to each ADC portion. In this case, the plurality of associated storage elements are represented by a plurality of associated registers $42_1 - 42_N$ (Gowda, Fig. 3) which are associated with a **respective** plurality of ADC portions $40_1 - 40_N$, and the converted digital value by each ADC portion is clearly stored into **one register (i.e., register 42_1) of the associated registers $42_1 - 42_N$.** Therefore, the Examiner respectfully submits that the independent claim 1 fairly reads on Gowda reference.

2. Applicant's arguments with respect to claims 5-7 have been considered and are persuasive. However, upon further consideration, a new ground of rejection is made without using Hayashi Kazou (JP 06-260938) reference (see section 4 below).

Additionally, since the Applicant does not traverse the Examiner's assertion of Official Notice of claim 7, the lack of traversal is an admission that the recited features are well known and thus the Official Notice taken to be prior art.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 3 & 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Gowda et al (US 6,115,066).

Regarding claim 1, Gowda discloses an active pixel sensor comprising:

an array of pixels (Fig. 3), arranged in logical units (columns C_1-C_N, or rows R_1-R_M), wherein each pixel comprises a photosensor element (30), an in-pixel buffer element (25, 23), and in-pixel selector element (22) (see Fig. 4 and col. 4, line 14 – col. 5, line 8);

a plurality analog-to-digital converters (40_1 – 40_N), formed on the same substrate as said pixel sensor array, and each associated with N logical units of the pixel sensor array (via column lines 15_1 – 15_N), each of N logical units having including a plurality of pixels (30) (see Fig. 3 and col. 4, lines 6-13), wherein

each analog-to-digital converter includes an ADC portion (40) which receives an analog signal from one of the pixel sensors of an associated logical unit when a selector element (22)

associated with one pixel is enabled, and converts said analog signal to a converted digital value indicating the output signal, and the ADC portion stores the converted digital value into one (i.e., 42_1) of a plurality of associated storage elements ($42_1 - 42_N$) and N is at least two (see Fig. 3; col. 3, line 53 – col. 5, line 8, and note that each of the A/D converters would be also tied to multiple columns lines 15).

Regarding claim 2, the logical units are lines of the array including either columns of the array or rows of the array (see Fig. 3; col. 3, lines 53-64).

Regarding claim 3, Gowda discloses that the analog-to-digital converters are associated with at least two adjacent lines of the array (see col. 4, lines 6-13 for each ADC associated with multiple column lines 15).

Regarding claim 8, each pixel is a CMOS pixel (see col. 1, lines 19-22).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al (US 6,115,066) in view of Adiletta (US 6,295,546).

Regarding claim 5, Gowda discloses a method for operating a pixel sensor array, comprising:

obtaining a pixel sensor array of photosensitive elements (Fig. 3), each having photosensitive element in a pixel, a buffer in the pixel (25, 23) associated with the photosensitive element, and a selector transistor in the pixel (22) which is enabled to allow a signal from the pixel to pass, and disabled to block the signal from passing (see Figs. 3 & 4 and col. 3, line 53 – col. 5, line 8);

connecting a plurality of said outputs of said selector transistors to one another, to form a plurality of logical units ($15_1 - 15_N$), each logical unit formed by a plurality of said output transistors (30) which are connected to one another (see Fig. 3);

receiving, in a plurality of A/D converter units (odd numbered ADC 40_1, 40_3, 40_5...), respective plurality of signals from a respective plurality of first logical units (odd numbered columns 15_1, 15_3, 15_5,...), and A/D converting said respective plurality of signals into a respective plurality of converted digital values and storing said respective plurality of converted digital values information in a respective first storage units (odd numbered registers 42_1, 42_3, 42_5,...) as shown in Fig. 3 and col. 3, lines 53-67;

receiving, in a plurality of A/D converter units (even numbered ADC 40_2, 40_4, 40_6...), respective plurality of signals from a respective plurality of second logical units (even numbered columns 15_2, 15_4, 15_6,...), adjacent to the first logical units, and A/D converting said respective

plurality of signals into a respective plurality of converted digital values and storing said respective plurality of converted digital values information in a respective second storage units (even numbered registers 42_2, 42_4, 42_6,...) as shown in Fig. 3 and col. 3, lines 53-67;

Gowda does not disclose that information in the A/D converters is read out in a different order than an order in which the information was converted.

Adiletta teaches a variation for reading out the digital image information from storage units in either little endian or big endian format for providing an appropriate output conversion format depending upon a requirement of a coupled device (see fig. 43B, col. 63, line 55 – col. 64, line 20).

Therefore, it would have been obvious to one of ordinary skill in the art to provide in Gowda an alternative readout method at the registers 42 in which the digital image information would be read out in either little endian or big endian format that is compatible upon requirements of a coupled device at the output 43 so that various image processing devices/storage devices of different formats are realized at the output of the image sensor.

Regarding claim 6, the little endian, big endian read out order taught by Adiletta is in a serial order.

Regarding claim 7, Gowda shows that said units are linear units which are one of rows and columns (see Fig. 3). Although Gowda and Adiletta do not explicitly disclose that the different order includes a first different order which skips lines between conversions, and a second different order which is a complete order, an Official Notice is taken that it is well known

in the art for reading out signals for processing in an imaging system by skipping lines between conversions in one order, and in a second order, it is a complete order.

Therefore, it would have been obvious to one of ordinary skill in the art to recognize that the combination of Gowda and Adiletta would be also implemented with a well known feature of skipping lines during readout from storage units in one order and a complete readout in a second order for signal processing.

Allowable Subject Matter

5. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to teach or fairly suggest the limitations "a readout controller, controlling readout information from the photosensor elements, by controlling said analog-to-digital converters to **each** convert information from a first line of the array, to store said information from the first line of the array in one of said plurality of associated storage elements, then to read out a second line of the array, and store information from said second line of the array in another one of said plurality of associated storage elements, and then to read out the information from all of the plurality of associated storage elements in a desired order.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

ANDREW CHRISTENSEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600